We claim:

sub #17

1. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal; and

a second PLL circuit generating a clock output signal, wherein said second PLL circuit is controlled by said bias signal generated by said first PLL circuit in a first mode and wherein said second PLL circuit has a second mode wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream.

2. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a transmission gate.

3. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a switch.

4. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a device that selectively imposes a bias current from said first PLL to said second PLL.

5. The clock recovery circuit of claim 1, wherein a transition between said first and second modes is controlled by a device that selectively imposes a bias voltage from said first PLL to said second PLL.

6. The clock recovery circuit of claim 1, wherein said first PLL circuit is tuned to a local clock that operates at substantially the same frequency as a transmitter clock.

7. The clock recovery circuit of claim 1, further comprising an elastic storage circuit for generating a jitter-compensated clock and data output.

8. The clock recovery circuit of claim 1, wherein said second mode is activated upon receipt of incoming data.

9. The clock recovery circuit of claim 1, wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data.

10. The clock recovery circuit of claim 1, wherein said input data stream is a bit packet in asynchronous transfer mode (ATM) format.

11. The clock recovery circuit of claim 1, wherein said first and second PLLs operate at different frequencies in accordance with one or more predefined ratios.

12. The clock recovery circuit of claim 1, wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data.

13. A method for recovering a clock signal from an incoming data stream, comprising:

tuning a first phase-locked loop (PLL) circuit to a local clock signal operating at substantially the same frequency as a transmitter clock, wherein said first PLL circuit produces a bias signal;

applying said bias signal to a second PLL circuit in a first mode, said second PLL circuit generating a clock output signal in said first mode having a frequency determined by said bias signal; and

removing said bias signal from said second PLL circuit in a second mode, wherein said second PLL circuit has an initial frequency in said second mode determined by said bias

signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes in said incoming data stream in said second mode.

14. The method of claim 13, wherein a transition between said first and second modes is controlled by a transmission gate.

15. The method of claim 13, wherein a transition between said first and second modes is controlled by a switch.

16. The method of claim 13, wherein a transition between said first and second modes is controlled by a device that imposes a bias current from said first PLL to said second PLL.

17. The method of claim 13, wherein a transition between said first and second modes is controlled by a device that imposes a bias current from said first PLL to said second PLL.

18. The method of claim 13, wherein said first PLL circuit is tuned to a local clock that operates at substantially the same frequency as a transmitter clock.

19. The method of claim 13, further comprising an elastic storage circuit for generating a jitter-compensated clock and data output.

20. The method of claim 13, wherein said second mode is activated upon receipt of incoming data.

21. The method of claim 13, wherein receipt of incoming data substantially instantaneously starts said second PLL in phase alignment with said received incoming data.

22. The method of claim 13, wherein said input data stream is a bit packet in asynchronous transfer mode (ATM) format.

23. The clock recovery circuit of claim 13, wherein said first and second PLLs operate at different frequencies in accordance with one or more predefined ratios.

24. The clock recovery circuit of claim 13, wherein said second PLL circuit generates said clock output signal using transmitted non-predetermined data.

25. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal; and

a second PLL circuit generating a clock output signal, wherein said second PLL circuit has an initial frequency determined by said bias signal and wherein said second PLL circuit substantially instantaneously adjusts said clock output signal to phase changes of data of an input data stream when said input data stream is present.

26. A clock recovery circuit, comprising:

first means for generating a first oscillator signal having substantially the same frequency as a transmitter clock;

means for generating a bias signal;

second means for generating a clock output signal having an initial frequency determined by said bias signal and substantially instantaneously adjusting said clock signal output signal to phase changes of data in an input data stream; and

means for selectively imposing said bias signal from said first means to said second means.

27. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a transmission gate.

28. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a switch.

29. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a device that selectively imposes a bias current from said first means to said second means.

30. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a device that selectively imposes a bias voltage from said first means to said second means.

31. The clock recovery circuit of claim 26, wherein said means for selectively imposing said bias signal is a multiplexer.

32. The clock recovery circuit of claim 26, further comprising means for generating a jitter-compensated clock and data output.

33. A clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal;

a second PLL circuit generating a clock output signal in accordance with a control input;

a phase detector for generating an error signal indicating a difference in phase between an incoming reference signal and said clock output signal; and

a multiplexer for selecting one of said bias signal and said error signal to apply to said control input.

34. The clock recovery circuit of claim 33, wherein said clock output signal corresponds to phase changes of data of an input data stream in a second mode when said input data stream is present.

35. The clock recovery circuit of claim 33, wherein said multiplexer selects said bias signal in a first mode so that said second PLL has an initial frequency determined by said bias signal.

36. The clock recovery circuit of claim 33, wherein said multiplexer selects said error signal in a second mode so that said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream.